

ABSTRACT OF THE DISCLOSURE

A multiple arbitration circuit capable of simultaneously arbitrating multiple paths from at least one source port to at least one destination port through a switch. The circuit comprises a crosspoint unit, and a multiple arbitration unit. The multiple arbitration unit comprises a request decoder, a prioritizer, a crosspoint select encoder and an acknowledge OR. The circuit operates such that if a source port is requesting a destination port that no other source port is requesting, then said requested destination port can be arbitrated simultaneously with requests by other source ports for other destination ports.

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